DISCONTINUITY EFFECTS ON HIGH FREQUENCY TRANSISTORS

Mohamed A. Megahed* and Samir M. El-Ghazaly
Telecommunications Research Center
Arizona State University. Tempe, Arizona 85287-7206
*Peregrine Semiconductor Corporation - San Diego office
San Diego, California 92121

ABSTRACT

The effects of input and output discontinuities on high frequency GaAs MESFET performance are analyzed. The transistor circuit, including both the active and passive elements, is evaluated using full-wave three dimensional physically based model. The S-parameters are simulated for different circuit topologies. Results clearly shows that the effect of these discontinuities is significant.

INTRODUCTION

In conventional high frequency GaAs transistors, several configurations are implemented. The layout of the physical device affects its performance, especially at high frequency of operation. The electrodes of the active device form a guided wave structure. At high frequency, those electrodes have to be treated as transmission lines. The transmission lines can be regarded as slot lines or coplanar waveguide, which forms a discontinuity at the input and output ports of the device. Therefore, the input and output impedance must be carefully analyzed. A common practice in analyzing the discontinuity effects on active devices is to analyze the passive structure separately from the behavior of the real active device [1]. This approach does not take into account the interaction between the wave propagating along the device electrodes and the electron transport in the active device and their effects on the device characteristics. On the other hand, it is very difficult to determine the discontinuity effects from measurement. First, disconnection and reconnection are sometimes necessary to switch a tuner to the a measuring device. Secondly, there usually is some physical distance between the FET and tuner. This situation prevents, in many cases, the possibility of matching the FET at all. Consequently, the true performance of the FET might be unknown.

In this paper, an algorithm, that deals with the electromagnetic wave and the electrodynamics inside the transistor simultaneously, is used to study the discontinuity effects on the high frequency performance of MESFET transistor. Although the method is difficult to formulate, it allows more accurate, flexible and realistic conditions to be investigated. The physical semiconductor model is based on the complete hydrodynamic system. The full-wave solution is used to update the ac fields inside the device. These two schemes are blended together using the current/field relation. The s-parameters are calculated for different device configurations.

0-7803-4603-6/97/$5.00 (c) IEEE

TRANSISTOR MODEL

The MESFET model used in this work is a full-wave three dimensional, physics based model. The model solves Maxwell's equation with the complete hydrodynamic system. The average electron density, energy, and velocity are obtained from the continuity, energy conservation, and momentum balance equations, respectively. The conduction current is directly calculated from the electron parameters. The displacement current is obtained from the full-wave scheme [2]. The transistor is analyzed in common source configuration, as shown in Fig. 1. The input and output ports are fully matched by applying the perfectly matched layer (PML) absorbing boundary conditions to truncate the computational domain. First, the dc transfer characteristics is calculated. Secondly, a suitable operating point is determined. The dc electron parameters are evaluated at the operating point. This procedure is required to initialize the semiconductor device. It resembles the initialization for time domain, or transient analysis, in circuit simulator. Then, an wide band ac excitation is launched at the input port of the transistor. The simulation proceeds and the output is collected from the output port of the transistor. The full-wave algorithm is based on the finite-difference time domain (FDTD) method. The physical semiconductor model is implemented using the finite difference approach with the first and second upwind scheme.

RESULTS AND DISCUSSIONS

The common source MESFET configuration can be regarded as two port network. The input is inserted at the input port between the gate and the source, while the output is collected at the output port between the drain and the source, and vice versa [4]. The transistor section is analyzed for different topologies of the MESFET transistor electrodes. Two configurations are considered, as shown in Fig. 3. The input and output feeding lines for the transistor determine the type of the transmission line. Fig. 3-a shows coplanar waveguides at both the input and output ports, named as (CP/CP). Fig. 3-b presents slot lines at both the input and output ports, described as (SL/SL). The slot line configuration represents a discontinuity between the feeding lines and the natural coplanar waveguide layout of the transistor electrodes. The discontinuity between the doped and undoped Si is always included in the analysis of the four configurations. The gate length of the transistor equals to 0.2 μm. The quiescent point is chosen at V_{ds}= 2V and V_{gs}= -1V. The device width is 150 μm. The channel and substrate doping equal to $2x10^{17}$ and $1x10^{14}$ cm^{-3}, respectively. The active layer thickness is typically 0.1 μm. The input and output terminals are extended for a distance of 30 μm. The reference planes are chosen far enough from the doped region. The scattering parameters are calculated for each structure. A wide band Rayleigh pulse, with amplitude of 0.05 V, is used as the ac excitation for the structure. The analysis is carried on in the frequency range from 5 GHz to 150 GHz to show the effects of the discontinuities on the value of the maximum frequency, f_{max}, of the transistor. The maximum frequency is defined in our analysis as the frequency where the transistor gain is unity. Fig. 4a-4b show the S-parameters calculated for the CP/CP configuration. Although this configuration is not practical, it serves the need for comparison with the actual topology. It is seen in Figs. 4a, that the reflection s-parameters, S_{11}, is considerably small since there is no discontinuities neither at the input nor at the output port of the active device. This shows that the amplifier is fairly stable under this topology condition. The transmission S-parameter, S_{21}, is

0-7803-4603-6/97/$5.00 (c) IEEE

shown in Fig. 4-b. The maximum frequency equals to 60 GHz. One must note that the devices described in our analysis are not optimized. Fig. 5a-5b present the S-parameters for the SL/SL configuration. The reflection S-parameter, S_{11}, is shown in Fig. 5a. The magnitude of S_{11} is larger than 0 dB at relatively low frequency. This means that the circuit configuration is unstable. . This can explained by the capacitive nature of the discontinuity at the output ports of the transistors. It can be considered as capacitance coupling between the gate and the drain, which represents a positive feedback element in the amplifier circuit. This will drive the amplifier circuits to instability regardless on the matching network at the input port of the transistor. S_{21} shows that the maximum frequency of this configuration is 130 GHz, as depicted in Fig. 5b. Also, the gain is higher than the CP/CP topology case. This behavior can be explained by the wave multiple reflection at both the input and output port discontinuities. The interaction between the wave propagating along the transistor electrodes and the electron transport inside the active device is obvious..

CONCLUSION

Full-wave three dimensional physically based device model is used to simulate the interaction between the electromagnetic wave propagating along the transistor transmission lines and the electronic transport inside the transistor. The discontinuities effects at the input and output ports of the transistor are studied. The S-parameters for different transistor layouts are simulated. Results show that the discontinuities along the transistor electrodes affects the stability of the transistor circuit.

ACKNOWLEGMENT

This work is supported by the Army Research Office under Contract No. DAAH04-95-1-0521 and computer time grant from Army High Performance Computational Research Center.

REFERENCES

[1] R. J. Akello, B. Easter, and I. M. Stephenson, " Effects of microstrip discontinuities on GaAs MESFET amplifier gain performance," Electronics Letters, vol. 13, no. 6, 1977, pp. 160-162.

[2] R. K. Hoffmann, Handbook of microwave integrated circuits. Norwood: Artech, 1987.

[3] M. Dydyk, " Master the T-junction and sharpen your MIC designs," Microwaves, no. 5, 1977, pp. 119-121.

[4] M. A. Alsunaidi and Samir M. El-Ghazaly, " Electron-wave interaction in submicrometer gate field effect transistors," in IEEE MTT-S Digest, 1995, pp. 1257-1260.

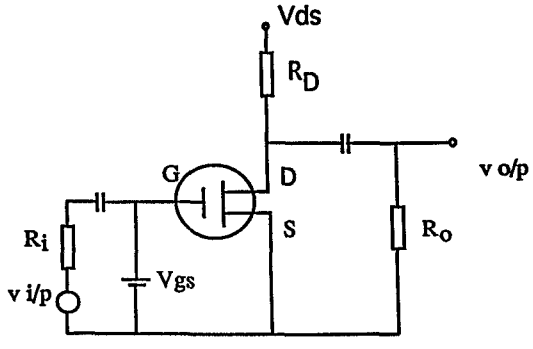

Fig. 1. Common source MESFET amplifier.

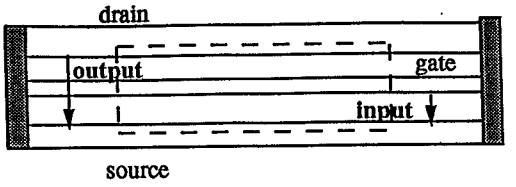

Fig. 2.a CP/CP Transistor topology.

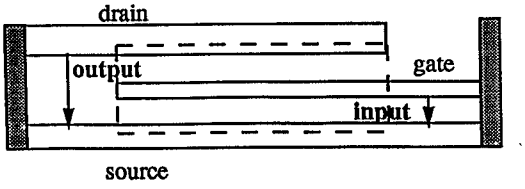

Fig. 2.b SL/SL Transistor topology.

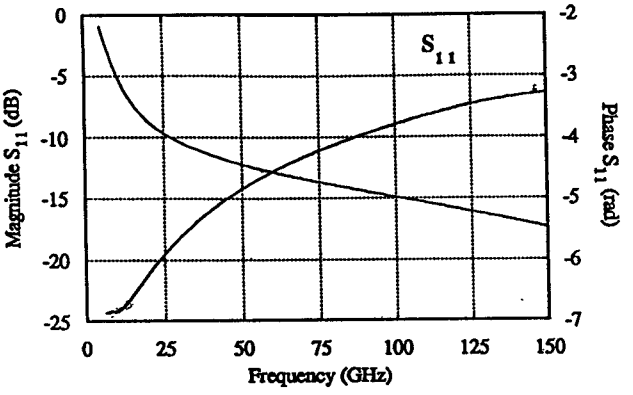

Fig. 3.a. Magnitude and Phase of S11 parameter for MESFET CP/CP topology.

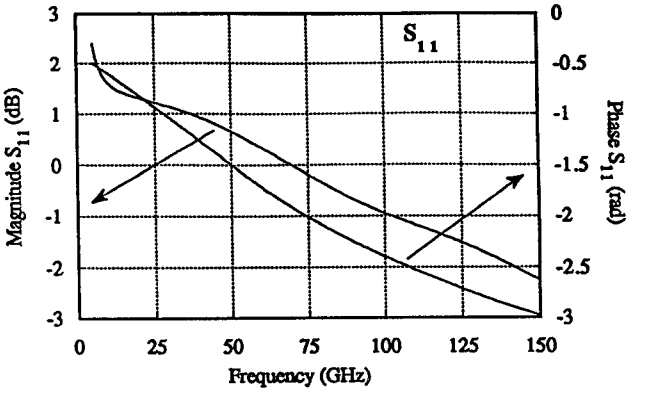

Fig. 4.a. Magnitude and Phase of S11 parameter for MESFET SL/SL topology

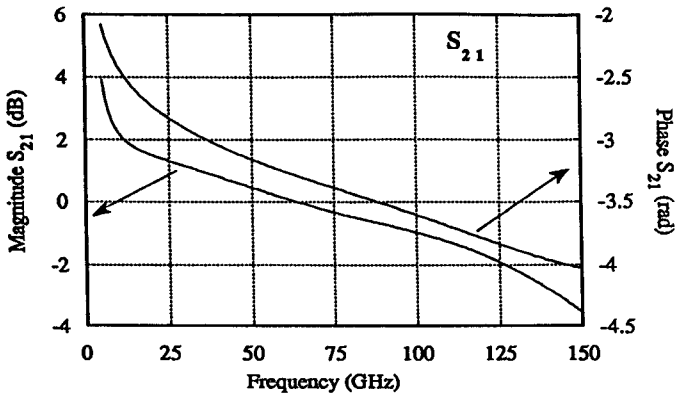

Fig. 3.b. Magnitude and Phase of S21 parameter for MESFET CP/CP topology.

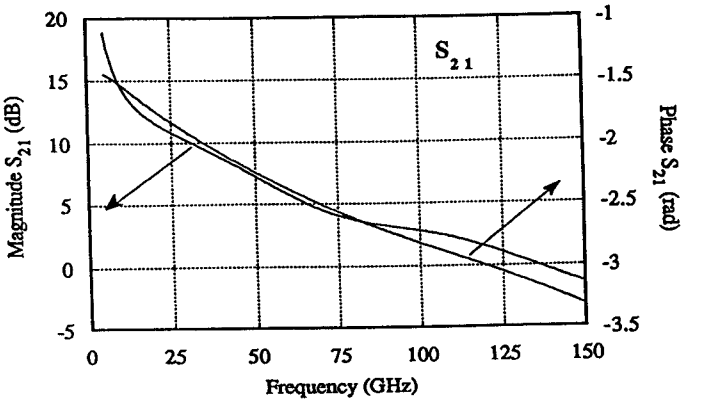

Fig. 4.b. Magnitude and Phase of S21 parameter for MESFET SL/SL topology.